REMARKS

Claims 1, 2, 5-11, and 16-23 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Chang et al., U.S. patent 6,347,380 and Lee et al., U.S. patent publication US 2004/0093443. Claims 3, and 4 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Chang et al U.S. patent 6,347,380 and Lee et al., U.S. patent publication US 2004/0093443 in view of Adamchick, U.S. patent 4,122,520. Claims 12-15 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Chang et al U.S. patent 6,347,380 and Lee et al., U.S. patent publication US 2004/0093443 in view of Lowe et al., U.S. patent 6,937,172.

Claim 1 has been amended to clearly recite functional limitations to accommodate the Examiner's assertions regarding intended use. Reconsideration of the claimed invention as described in the specification, and as recited in the independent claims 1 and 16, as presented, and dependent claims 2-15, and 17-23, is requested. Applicants respectfully submit that each of the pending claims 1-23 are patentable over all of the references of record.

Hsu et al., U.S. patent publication US 2003/0177295 discloses apparatus and method for controlling an asynchronous First-In-First-Out (FIFO) memory. The asynchronous FIFO has separate, free running read and write clocks. A number of n-bit circular Gray code counters are used to handshake the operation between read and

write parts of the FIFO, wherein n is any integer more than one. Additional binary counters are used to accumulate the read and write overflows for the circular Gray code counters. When any circular Gray code counter is overflow, the read or write count is transferred to the respective binary counter for recording the FIFO accesses. As set forth at paragraph 24:

> [0024] FIG. 5 illustrates the asynchronous dual port FIFO 500 in accordance with the invention. The asynchronous dual port FIFO 500 comprises a dual port random access memory (RAM) 510. Input data are written into the RAM 510 through an input port (not shown) and a write pointer Wptr indicates a write address. Output data are read from the RAM 510 through an output port (not shown) and a read pointer Rptr indicates a read address. The FIFO 500 further comprises a pair of read and write parts with symmetrical implementation. Each part contains an FIFO status indicator (501, 502), a handshaking unit (503, 504), and an overflow controller (505, 506). The FIFO status indicator (501, 502) indicates the levels of the RAM 510 use in an FIFO pointer and the read or write pointer (see FIG. 8). The level of the RAM 510 use in the FIFO pointer can state the FIFO full with FULL (see FIG. 8) in the write part and the FIFO empty with EMPTY in the read part. Each pointer is a binary counter. The handshaking unit (503, 504) contains two n-bit Gray code counters and a synchronizing circuit (see FIG. 6), wherein n is any integer more than one. The synchronizing circuit can be an Flip/Flop. The overflow controller (505, 506) cooperates with the handshaking unit to obtain the performance of FIG. 4. As cited, the performance is identical to both read and write parts. For simplicity, the further description only gives to the write part as shown in FIGS. 6 to 8.

Chang et al., U.S. patent 6,347,380 discloses a phase locked loop that is employed to provide a clock signal for controlling the reading or writing of audio data from or into a memory to avoid memory overflow and underrun. The difference between the write and read pointers is monitored and used for adjusting a divider counter used in the feedback loop of the phase locked loop, by incrementing, decrementing by one or leaving unchanged the value of the counter. The counter is used to divide the output of the phase locked loop to provide a reference signal to the

phase locked loop. A reference frequency for reading the audio data may be set close to the writing speed by incrementing or decrementing the reading speed by fine adjustment steps until the reference frequency is reached. After the reference frequency is reached, the reading speed is changed between the reference frequency and a frequency one fine adjustment step away from the reference frequency so that the average reading speed is equal to the writing speed.

Lee, U.S. patent publication US 2004/0093443 discloses apparatus for effectively and economically receiving packet by eliminating temporal memory and controller. The apparatus includes; an inspection logic circuit for inspecting data units as soon as arrived in order to find error included in the packet and generating control signals according to a result of inspecting data unit; a multiplexer for receiving data units and distributing the received data units as soon as the data units are arrived; and a plurality of FIFO memories for receiving the data unit, storing the data unit in corresponding one of FIFO memories and deleting or completing to store data units according to the control signals from the inspection logic circuit. The present invention can reduce manufacturing cost of the apparatus by eliminating a temporal memory and a memory controller for the temporal memory and can also reduce a processing time.

Adamchick, U.S. patent 4,122,520 discloses a microcomputer controller for a printer, and apparatus for facilitating direct memory access to the microcomputer, includes a central processing unit (CPU) with a known set-up time at the beginning of each machine cycle. A memory, associated with the CPU, has an access time less than the CPU set-up time. A pair of three-state buffers are utilized on the address bus

to, and the data bus to and from, the memory from each of the CPU and a direct memory access (DMA) port. A DMA control circuit is coupled to the three-state buffers to facilitate direct access to the memory, from the DMA port, during CPU set-up time intervals and also returns control of memory access to the CPU when the set-up, or synchronization, time interval ends. The microcomputer controller is utilized with additional memory, of the read-only type, and shift registers for realizing a printer controller capable of receiving print character data from the DMA port and causing that data to be printed as the associated symbol, indicia and the like, in a print font selected responsive to incoming data.

Lowe et al., U.S. patent 6,937,172 discloses a system for gray-code counting in an integrated circuit such as a programmable logic device uses a binary adder coupled to a binary counter output and to a selected binary offset value. The binary adder provides a binary sum that is converted to a gray code value by a binary-to-gray converter. The gray code value represents the binary sum output. FIG. 9D is a simplified flow chart of a method 990 for Gray-code counting in a programmable logic device. FIG. 8 illustrates an example of a circuit suitable for performing this method. A selected pointer offset binary value is added to a pointer count binary value to produce a binary sum (step 991). The binary sum is converted to a Gray-code value (step 992), and the Gray-code value is coupled to a first port of a multiplexer (step 993). The multiplexer output is coupled to a register input (step 994), and the register output is coupled (fed back) to a second port of the multiplexer (step 996). The pointer count binary value is incremented in response to a pointer increment signal to create an

incremented Gray-code value (step 997), and the incremented Gray-code value is coupled through the multiplexer when the pointer increment signal is asserted (step 998), and the register output is coupled through the multiplexer when the pointer increment signal is not asserted (step 999).

Applicant respectfully submits that the total teachings of Hsu et al., Chang et al., and Lee et al. do not achieve, nor suggest, the subject matter of the invention as expressly recited in independent claims 1, and 16, as presented. Applicant respectfully submits that there is no teaching or suggestion in any of the cited references, individually or taken as a whole, to make the claimed invention obvious.

Reconsideration and allowance of each of the pending claims 1-23, as presented, is respectfully requested.

35 U.S.C. §103 requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966).

Applicants respectfully submit that independent claims 1, and 16, as amended, are patentable over the references of record including the Hsu et al., Chang et al., and Lee et al. Independent claims 1, and 16 respectively recite a flow through asynchronous elastic first-in, first-out (FIFO) apparatus and a method for implementing multi-engine parsing and authentication with a flow through asynchronous elastic first-in, first-out (FIFO) apparatus.

The flow through asynchronous elastic first-in, first-out (FIFO) apparatus of independent claim 1 is defined: a FIFO random access memory (RAM) having a data

input for receiving data and control information and a data output for outputting said data and control information; write clocked logic for loading said data and control information to said FIFO RAM at a first clock frequency; asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at a second clock frequency; one of said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for outputting said data and control information from said FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency.

The method of independent claim 16 further define the steps of: loading data and control information to the FIFO RAM at a first clock frequency; outputting said data and control information from the FIFO RAM at a second clock frequency.

Only Applicants teach a flow through asynchronous elastic FIFO apparatus that passes data and control information through the asynchronous FIFO RAM. Thus, as only taught by Applicants, enabling other higher level functions, such as, interleaving multiple direct memory accesses (DMAs), and providing a clean abort/discard data function. (See page 5, starting at line 12 of the specification.) Neither Hsu et al., Chang et al., nor Lee et al. provides any remote suggestion of loading control information into the FIFO RAM. Hsu et al. provides no motivation, suggestion or teaching to support the Examiner's assertion that the FIFO random access memory (RAM) having a data input for receiving data and control information and a data output for outputting said data and control information. Applicants respectfully submit that claims 1, and 16, are patentable.

In order for there to be a prima facie showing of obviousness under 35 U.S.C. §103, applicants' claimed invention which must be considered as a whole pursuant to 35 U.S.C. §103, and failure to consider the claimed invention as a whole is an error of law. Applicant respectfully submits that when the recited limitations of the claims 1 and 16, as presented, are considered as a whole, the prior art references of record can not be combined to establish a prima facie showing of obviousness. The mere fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. A combination of all the teachings of the references of record would not achieve the claimed invention as recited by claim 1.

Contrary to the Examiner's assertions set forth in rejection of claim 1, Hsu et al. do not suggest that data and control information are all stored into the RAM. Only Applicants teach, as set forth at page 7, starting at line 7 that data and control information are all stored into the RAM 102 instead of just data. An exemplary Data Field and a plurality of exemplary Control Fields are illustrated and described with respect to FIG. 3.

A prior art reference may be considered to teach away when "a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.

Applicants respectfully submit that one of ordinary skill in the art would not have been led to the claimed invention by the reasonable teachings or suggestions

found in the prior art, including Hsu et al., Chang et al., and Lee et al.

Only Applicants teach a FIFO RAM with one of said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for outputting said data and control information from said FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency.

Hsu et al. teach the use of a pair of n-bit circular Gray code counters for handshaking read-out and write-in operation frequencies in the dual port FIFO memory and an n-bit overflow binary counter for accumulating overflows of the pair of n-bit circular Gray code counters, wherein n is any integer more than one.

Chang et al. teaches a phase locked loop control arrangement with adjustments away from the reference frequency so that the average reading speed is equal to the writing speed.

Lee et al. teaches a plurality of FIFO memories for receiving the data unit, storing the data unit in corresponding one of FIFO memories and deleting or completing to store data units according to the control signals from the inspection logic circuit.

Applicants respectfully submit that the total teachings of Hsu et al., Chang et al. and Lee et al. do not show, nor suggest a FIFO RAM for storing control information, as taught and claimed by independent claim 1. Applicants respectfully submit that the total teachings of Hsu et al., Chang et al. and Lee et al. do not show, nor suggest a FIFO RAM with one of said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for

outputting said data and control information from said FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency, as taught and claimed by Applicants.

The above features of the flow through asynchronous elastic first-in, first-out (FIFO) apparatus and a method for implementing multi-engine parsing and authentication as taught and claimed by Applicants in independent claims 1, and 16, as amended, are neither disclosed, nor remotely suggested, in Hsu et al. and Chang et al.

Hsu et al. teach storing data and considering the total teachings of Hsu et al., Chang et al. and Lee et al. no teaching, suggestion, nor any motivation is provided for storing data and control information into a FIFO RAM as taught and claimed by Applicants.

Considering the total teachings of Hsu et al., Chang et al. and Lee et al. no teaching, suggestion, nor any motivation is provided for one of said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for outputting said data and control information from said FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency, as taught and claimed by Applicants.

It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements. Rejections based on § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art.

Thus, each of the independent claims 1, and 16, as amended, is patentable.

Dependent claims 2-15, and 17-23 respectively depend from patentable independent claims 1, and 16, as amended, further defining the invention. Each of the dependent claims 2-15, and 17-23 is patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-23, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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